1.1 Scope.

This specification covers the requirements for a flash 10-bit, 75 Msps TTL analog-to-digital converter (ADC). Refer to the commercial data sheet for applications information.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD9060S(X)/883B
−2	AD9060T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-68A	68-Pin Leadless Ceramic Chip Carrier
Z	Z-68	68-Pin Leaded Ceramic Chip Carrier

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Positive Supply Voltage ($+V_S$) ..... +6 V
Negative Supply Voltage ($-V_S$) ..... −6 V
Analog Input Voltage ..... −2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ ..... −2 V to +2 V
$+V_{REF}$ to $-V_{REF}$ ..... 4.0 V
ENCODE, $\overline{\text{ENCODE}}$ ..... 0 V to $-V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current ..... ±10 mA
Digital Output Current ..... 20 mA
Operating Temperature Range (Case) ..... −55°C to +125°C
Junction Temperature ..... +175°C
Storage Temperature Range (Case) ..... −65°C to +150°C
Lead Soldering Temperature (10 sec) ..... +300°C

1.5 Thermal Characteristics.

Maximum junction temperature should not be allowed to exceed +175°C. Typical thermal impedances (part soldered onto board):

68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow);
θ_{JA} = 15°C/W (air flow = 500 LFPM)
68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow);
θ_{JA} = 13°C/W (air flow = 500 LFPM).

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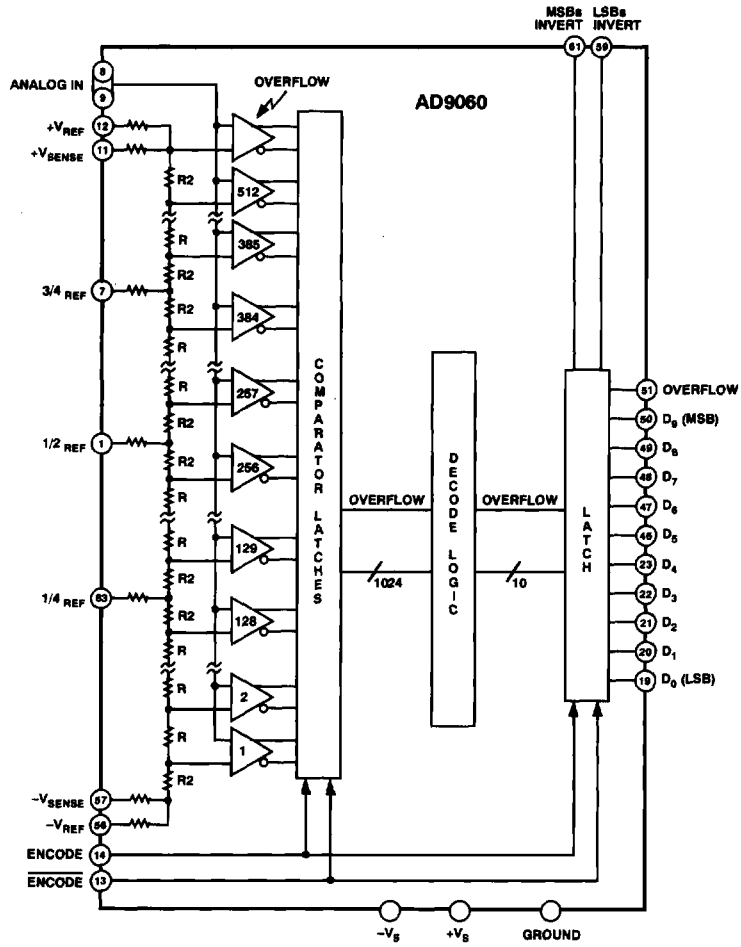
Table 1.

Test	Symbol	Device	Design Limits[1]	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions[2]	Units
Differential Nonlinearity	DNL	−1					1.25	1.5		See Note 3	LSB
		−2					1.0	1.25			
Integral Nonlinearity	INL	−1					2.0	2.5		See Note 3	LSB
		−2					1.5	2.0			
No Missing Codes		All					Guaranteed See Note 3				
Input Bias Current	I_B	All		1	2					See Note 4	mA max
Input Resistance	R_I	All		2.0							kΩ min
Reference Ladder Resistance	R_{RL}	All		22	14						Ω min
				56	66						Ω max
Reference Ladder Offset (Top)	O_{RLT}	All					90	90			mV max
Reference Ladder Offset (Bottom)	O_{RLB}	All					90	90			mV max
Maximum Conversion Rate		All				75					Msps min
Output Delay	t_{OD}	All							2	See Note 5	ns min
									9		ns max
Output Time Skew	t_{OTS}	All							3	See Note 5	ns max
Rise Time	t_R	All							3		ns max
Fall Time	t_F	All							3		ns max
Encode Pulse Voltage (HIGH)	$V_{E(H)}$	All		−1.1	−1.1						V min
Encode Pulse Voltage (LOW)	$V_{E(L)}$	All		−1.5	−1.5						V max
Encode Pulse Current (HIGH)	$I_{E(H)}$	All		300	300						μA max
Encode Pulse Current (LOW)	$I_{E(L)}$	All		300	300						μA max
Encode Pulse Width (HIGH)	$t_{E(H)}$	All				6					ns min
Encode Pulse Width (LOW)	$t_{E(L)}$	All				6					ns min
Effective Number of Bits	ENOB	All				8.7				A_{IN} = 2.3 MHz	Bits min
Signal-to-Noise Ratio[6]	SNR	All				54				A_{IN} = 2.3 MHz	dB min
						51				AIN = 10.3 MHz	dB min
						44				A_{IN} = 15.3 MHz	
Signal-to-Noise Ratio[7]	SNR	All				54				A_{IN} = 2.3 MHz	dB min
						51				A_{IN} = 10.3 MHz	dB
						46				A_{IN} = 15.3 MHz	dB min
Harmonic Distortion	HD	All				61				A_{IN} = 2.3 MHz	dBc min
						55				A_{IN} = 10.3 MHz	dBc min
						47				A_{IN} = 15.3 MHz	min
High Level Output Voltage	V_{OH}	All		−1.1	−1.1						V min
Low Level Output Voltage	V_{OL}	All		−1.5	−1.5						V max
$+V_S$ Supply Current	$+I_S$	All		500	500						mA max
$-V_S$ Supply Current	$-I_S$	All		180	190						mA max
Power Dissipation	$-I_S$	All		3.3	3.5						W max
Power Supply Rejection Ratio	PSRR	All					10	10			mV/V max

NOTES
[1]Value shown is over full temperature range. Number in this column indicates specification is guaranteed but not tested.
[2]$\pm V_S = \pm 5$ V; $\pm V_{SENSE} = \pm 1.75$ V; ENCODE = 40 Msps, unless otherwise indicated.
[3]3/4 REF, 1/2 REF, and 1/4 REF reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Accuracy of the overflow comparator is not tested and is not included in linearity specifications.
[4]Measured with ANALOG IN = $+V_{SENSE}$.
[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D0–D9. Output skew measured as worst-case difference in output delay among D0–D9.
[6]RMS signal to rms noise, including harmonics, with analog input signal 1 dB below full scale at specified frequency.
[7]RMS signal to rms noise, without harmonics, with analog input signal 1 dB below full scale at specified frequency.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).